Simulation and Analysis of SVHM Technique for DCMLI under Transient Conditions with Non-Linear Loads

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Abstract –This paper presents the simulation and analysis of space-vector hysteresis modulation (SVHM) technique for three-level Diode Clamped Multilevel Inverter (DCMLI) under transient conditions with Non-Linear Loads. The ultimate aim of the paper is, this modulation technique is to force the actual current to reach the reference current and, simultaneously, balance the capacitor voltages. The SVHM method permits for the efficient application of zero voltage vectors and avoids high switching frequencies triggered by phase interaction in DCMLI. The effectiveness of the proposed system is proved with the help of simulation. The simulation is performed in MATLAB/Simulink. From the simulation results, it shows that the proposed multilevel inverter works properly to generate the multilevel output waveform with minimum number of semiconductor devices and to achieve high dynamic performance with low THD with transient conditions and also balance the capacitor voltages.

Index Terms –Space Vector Hysteresis Modulation (SVHM), Diode Clamped Multilevel Inverter (DCMLI), Non-linear Loads, Transient conditions

1. INTRODUCTION

Today, the energy demand is moving on increasing toward generating power with renewable energy source that may be dispersed in a wide area, and most of them are renewable, as they have greater advantages due to their environmentally friendly nature. Photovoltaic (PV) energy has augmented interest in wide range of electrical power applications, since it is considered as a basically limitless and generally on hand energy resource with the focus on greener sources of power particularly for distant locations where utility power is engaged [1-4]. The solar can be used by all in universe which doesn't need more investigations of producing electricity [5-7]. This leads to research in multilevel inverters.

The fast increasing use of power-electronics equipment in recent years has increased the number of nonlinear loads that draw harmonic currents from the power system [8]. The undesired current components cause stress to the power system, generating disturbed fundamental and harmonic voltage drops in the network impedances. They may add additional losses and even excite resonances [9-14]. The active power filter is a common approach to eliminate the undesired current components by injecting equal but opposite harmonic currents [15-18]. Active filtering can be based on various control strategies for obtaining the compensator current reference values, working either in the frequency domain or in the time domain.

Multilevel inverters [19-22] are becoming an established means for developing new high-power applications that require substantial increase of both current and voltage magnitudes. The advantages of multilevel inverters have been well known since the first NPC inverter was proposed in [23-25]. This particular topology increases the power rating because the blocking voltage of each switch is one-half of the dc-bus voltage. Moreover, their output-voltage harmonic content is much smaller than that of two-level inverters with the same switching frequency owing to the output-voltage waveform improvements [26].

The multilevel inverters are classified into three types namely: (i) Diode clamped multilevel inverters; (ii) Flying capacitor multilevel inverter; and (iii) Cascaded H bridge multilevel inverter. Of these the cascaded H bridge multilevel inverter topologies give better results. The research goes on increasing to propose a new structure of inverter with reduced semiconductor devices with increased multilevel at the output waveform [27-33]. The study of the multi sampled multilevel inverters and their control techniques to improve the performance of the multilevel inverters. This also deals with the different control techniques to be implemented in multilevel inverters in order to reduce the total harmonic distortion (THD). But they don't concentrate on the structure of the multilevel inverters [34-38].

A way to balance the capacitor voltage to produce voltage levels of equal width. Therefore the THD is reduced. There is no change in the structure of the inverter. Only the technique has been implemented with conventional structure but they achieved better THD [39-45]. The new algorithm for producing the switching signals. Here new optimization algorithm to produce the modulation signals; the algorithm works better than the other techniques but the structure of cascaded multilevel inverter remains same. Hence the switching loss is more and the number of switches used is same as that of the conventional one. Therefore it is necessary to find the new structural way of producing multilevel with reduced semiconductor devices [46-52].

The cascaded H bridge topology to be used, to reduce THD and the multilevel inverter fed multiphase induction motor; here they use diode clamped inverter to produce multiple levels at the output and they are used to drive the five phase motor. The performance analysis is done using this. Since they use diode clamped multilevel inverter the number of semiconductor devices is high and hence the losses are heavy. On replacing it with a new structure and by increasing the number of levels can improve the performance of the system [53-54]. The closed loop control strategy implemented in multilevel inverter is explained and the control circuit is also big which again increases the circuit complexity thus reducing the effectiveness of the proposed system [55-56].

From all the above analysis, conclude that, the proposed technique is designed based on the following steps: combining three error currents into a single space-vector, constructing two alternative hysteresis strategies in stationary reference frame around the error vector tip, detecting the region and the segment in which the error vector tip is located, and selecting a suitable voltage vector to bring the error vector back within the hysteresis boundaries and, at the same time, balance the capacitor voltages. Two case studies are considered here to evaluate the performance of the proposed modulation technique when applied to DCMLI systems.

2. CURRENT CONTROL METHODS

This paper discusses current control methods for shunt active power filter. Reference current is predicted from the FFT algorithm. That reference current is used for current control methods. Following methods are reported in literature for current control of shunt active power filter.

- PI based current control

  (Carrier based current control)

- Space Vector Hysteresis Current Control

  (Carrier less current control)

2.1 PI based Current Control:

However, parameters of PI controllers must be carefully tuned with a trade-off between maintaining the system stability over the whole operation range and achieving an adequate dynamic response during transients. This can result in degraded transient performance, which in turn, hinders the application of PI current controller in high-demanding situations, such as active power filters. This method is also called Sine Pulse Width Modulation method for shunt active power filter with triangular carrier wave. It can limit switching frequency of inverter. It will degraded transient performance of filter.

2.2 Space Vector Hysteresis Current Control for Three-level VSI:

Fig. 1 Shows the Space Vector current control, in stationary αβ-coordinates based on the five-level hysteresis comparator. Based on current error five-level hysteresis comparators will give values of dα and dβ.

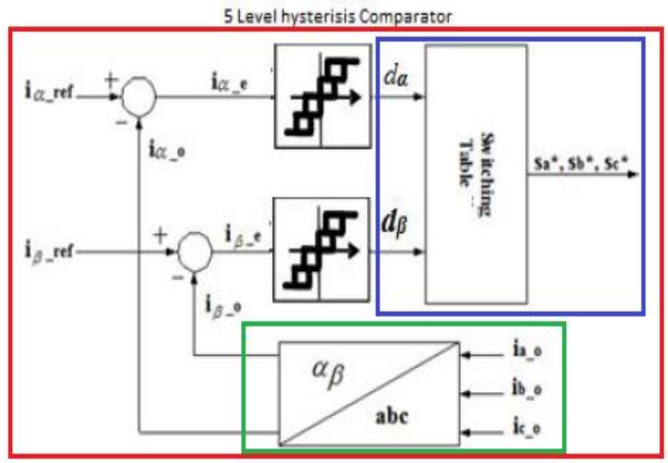

Fig.1 Five level Hysteresis comparator for three-level VSI

The switching states of the three-level inverter can be represented in the αβ-coordinates, as shown in Fig. 2. Based on the values of dα and dβ, the appropriate voltage vectors are selected.

From this survey it is concluded that PI based current control methods can limit the switching frequency of inverter. Space vector based current control method cannot limit the switching frequency. Space vector based current control method is complex for three level inverter based shunt active power filter.

3. ACTIVE POWER FILTER FOR NON-LINEAR LOADS

Fig. 3 shows the topology of an APF configuration. This topology is composed of a DCMLI attached to the point of common coupling (PCC) through a first-order low pass filter. Active power filter is controlled such that it removes the load current harmonics and supplies load reactive power to accomplish harmonic-free source currents at unity power factor. In the steady state, the active power supplied from the power network must be equal to the required load power.

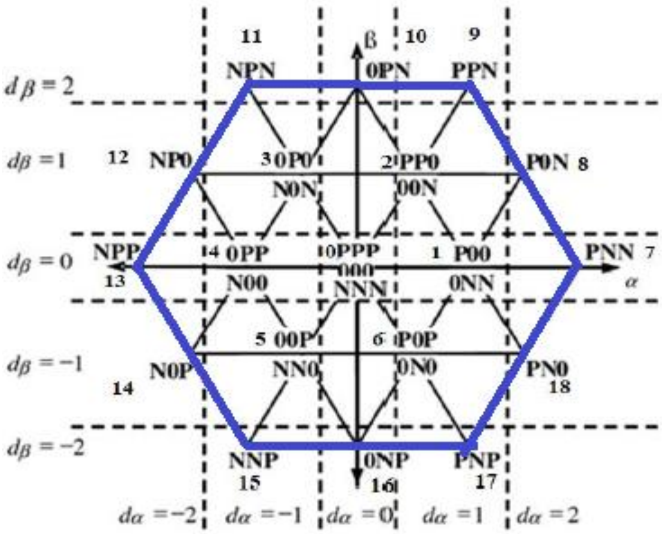

Fig.2 Space-vector diagram for three-level inverter

However, the active power balance between the power network and the load will not be kept if any change happens to the load power. This transient will deviate the average voltage of the dc-bus voltage away from the reference voltage. Therefore, the amplitude of the source current must be adjusted in order to keep the active power filter operation satisfactory. The active power provided by power network is formerly altered similarly to compensate the active power supplied/received by the dc-bus capacitor and match the active power used by the load.

4. SPACE VECTRO HYSTERESIS MODULATION TECHNIQUE

Three-Level Half-Bridge DCMLI Inverter Fig. 3 shows the configuration of a DCMLI inverter. It is assumed that the upper-leg and lower-leg capacitor voltages are identical and equal to $V_{dc}/2$. To have a correct operation, the proposed modulation technique has to produce the correct voltage vector to keep the inverter current within the hysteresis boundaries, create proper multilevel voltages and, simultaneously, balance the capacitor voltages.

Fig. 4 shows the proposed switching technique of the DCMLI inverter-based active power filter. As observed, it comprises of four units, a measurement unit, an error computation unit, an region and segment detection unit and a voltage vector selection unit.

To produce the switching signals, the output currents initially need to be measured. This procedure is performed in the measurement unit. Then, the output currents along with the reference currents obtained from the reference current circuit are transferred to stationary reference frame. Here, the error vector can be calculated simply by subtracting the reference current from the measured current in stationary reference frame.

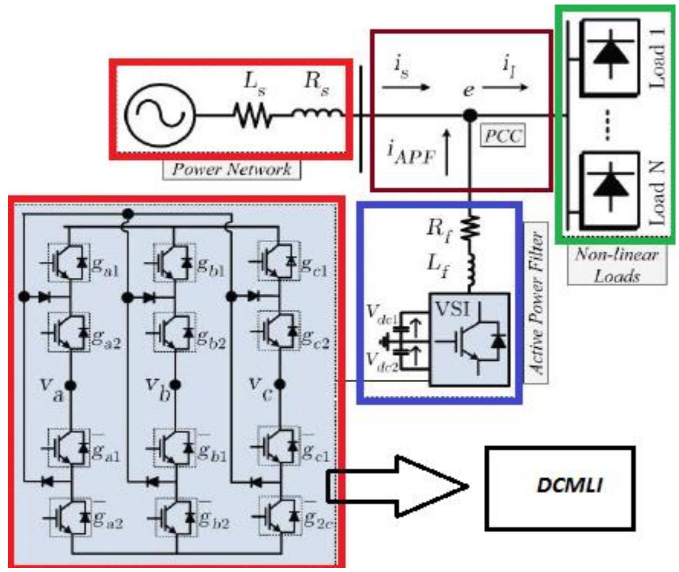

Fig. 3 APF compensation principle

By defining the error vector magnitude and angle, the region and segment detection unit can define the segment where the error vector resides. After this step, the proper voltage vector is selected using the voltage vector selection unit. As mentioned earlier, apart from keeping the error vector within the hysteresis boundaries and produce correct multilevel voltages, the proposed technique must be able to balance the capacitor voltages as well. To do this, two alternative hysteresis strategies have been taken into account. The first strategy is designed with the purpose of utilizing the medium and large voltage vectors to keep the error vector within the hysteresis boundaries, while the second one is developed according to the small-voltage vectors to balance the capacitor voltages. It is to be noted that this modulation technique is designed with inspiration of the method proposed.

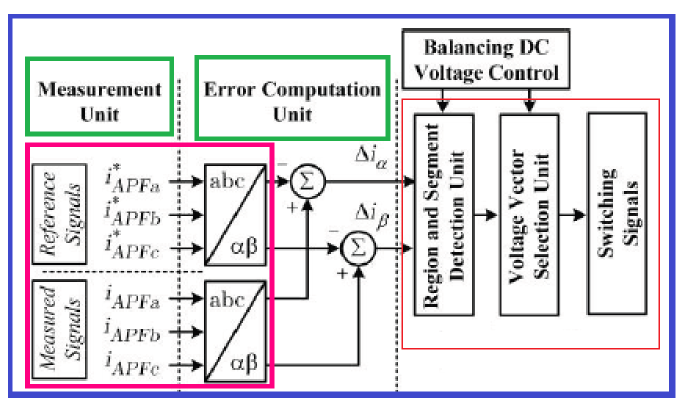

Fig. 4 SVHM modulation technique.

5. REGION AND SEGMENT DETECTION AND VOLTAGE VECTOR SELECTION UNIT

The tip of the reference current vector moves on a circle around the origin of the coordinate system. The analysis is performed in stationary reference frame; hence the transformation of the three hysteresis-bands into this frame results in two circular hysteresis-bands and three regions in total. These regions are chosen in order to use the zero, medium and large voltage vectors, when the capacitor voltages are balanced and the zero and small-voltage vectors, when the capacitor voltages are unbalanced. The conditions that require to be met for the error vector to reside in each particular segment to charge and discharge the capacitors when the capacitor voltages are unbalanced. When the error vector tip is located in region, the error vector magnitude is small and measured satisfactorily within the required accuracy for tracking the reference current. The error vector magnitude is small and measured satisfactorily within the required accuracy for tracking the reference current. Then, one of the three zero-voltage vectors closest to the previous switching is applied, and no connection is made.

6. CREATION OF THE REFERENCE CURRENT

The outer loop of the control system provides the reference current for the inner current loop is shown in Fig.5. The outer loop includes a slow PI controller to regulate the DC voltage and a reference current calculation unit. As shown, the active filter provides the entire load current minus the positive-sequence fundamental current necessary to supply the active power in the load and the losses in the active filter. The positive-sequence fundamental current required from the system is calculated from the average required power (p), divided by the positive-sequence system voltage. A one cycle sliding window DFT calculates the average positive sequence system voltage.

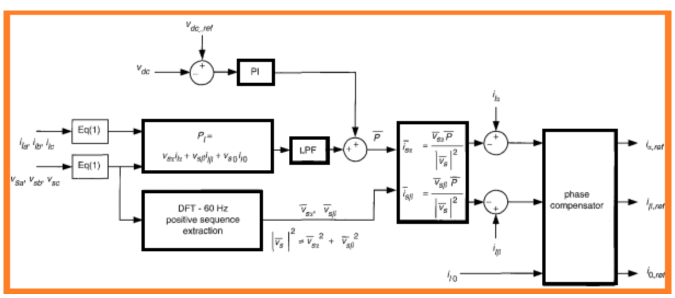

Fig. 5 Inner current loop.

It should be noted that the two sampling periods delay can cause a significant phase difference between the reference and actual currents, especially at harmonic frequencies. To overcome this problem, an equal but opposite phase shift is added to the reference. This task is performed in the phase compensation unit.

7. SIMULATION RESULTS

To verify the performance of the proposed modulation technique, four case studies are considered in this paper. The system parameters are L_{filter}=10.10mh, C_1 and C_2=2810 micro farad and V_{ac}=110V.

7.1 Transient Performance of SVHM for a Grid Connected NPC Inverter:

In this case, the transient performance of the proposed SVHM strategy is investigated for the grid connected DCMLI inverter. Figs. 6(a-d) depict the simulation results including the reference signals, the inverter currents, the phase-a inverter voltage and the dc-bus voltage. Figs. 6(b) and 6(d) show that the actual inverter currents and the dc-bus voltage follow their references quickly after the reference change verifying the effectiveness of the proposed technique in transient conditions.

7.2 Transient Performance of SVHM for an APF Compensating Non-linear Loads:

Here, the structure of Fig. 3 is simulated for a transient condition (a sudden load change, i.e., a 100% increase shown in Fig. 7(a)). As can be comprehended in Figs. 7(a-f), the phase-a active power filter current follows its reference and compensates the load current very quickly after the load change. The harmonic spectrums of the source current before and after load change are shown in Fig. 7(e) and Fig. 7(f), respectively. The THD percentage of the source current is kept lower than 5%, which is the standard value in the distribution level, while the THD percentage of the load current is 27%.

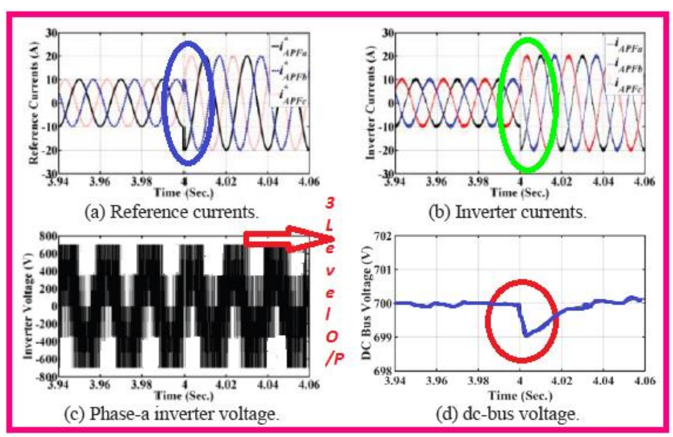

Fig 6 DCMLI Inverter producing the reference signals using SVHM under transient.

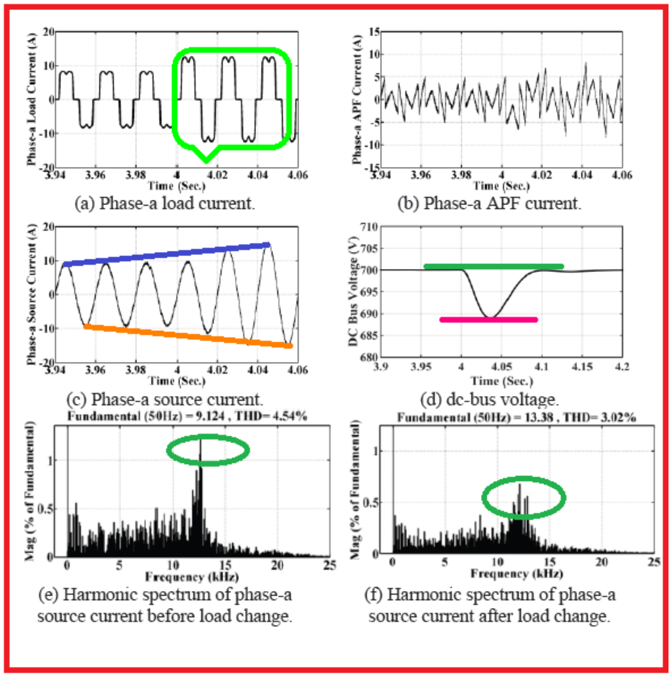

Fig. 7. APF compensating nonlinear loads using SVHM under transient.

These figures also verify the proposed technique capability in avoiding high switching frequencies triggered by phase interaction due to the floated neutral point of DCMLI.

8. CONCLUSION

This paper presents a new SVHM approach implemented in stationary reference frame. The application is the three-level DCMLI -based active power filter. The procedure has been done in stationary reference frame by converting the three error-currents to a single vector that can be located in 12 segments of the first hysteresis strategy associated with the zero-, medium- and large-voltage vectors and 6 segments of the second hysteresis strategy associated with the zero- and small-voltage vectors for balanced and unbalanced capacitor voltages, respectively. As a result, the inter phases dependency, which causes high switching frequency in DCMLI systems, is prevented. The validity of the proposed method is shown through extensive simulation investigations applied to DCMLI systems for both the steady state and transient conditions.

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